UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,218	09/21/2000	Jae-hun Lee	SAM-143	9230

		EXAMINER
7590	07/31/2006	TRAN, TRANG U

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2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/666,218	LEE ET AL.
	Examiner	Art Unit	
	Trang U. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>01 May 2006</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 19-24* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,8,9,19,20,23 and 24* is/are rejected.

7)☒ Claim(s) *3-5,7,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments with respect to claims 1-9 and 19-24 have been

considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 101

2.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
> matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
> conditions and requirements of this title.

3.   Claims 23-24 are rejected under 35 U.S.C. 101 because claims 23-24 are not a

new and useful process, machine, manufacture, or composition of matter, The claimed

a method of restoring information data has **no practical application of the §101**

judicial exception and are seeking to **pre-empt the use of claimed method**.

The examiner suggests clarifying the claimed practical application so as to

exclude recitation of every "substantial practical application" of the claimed law of

nature. Any amendment to the claim should be commensurate with its corresponding

disclosure.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1, 6, 8-9, 19-20 and 23 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Suemura et al (US Patent No. 5,887,039) in view of Danger (US

Patent No. 5,633,608).

In considering claim 1, Suemura et al discloses all the claimed subject matter,

note 1) the claimed a video controller for separating color signals and a

horizontal/vertical synchronous signal from an original video signal, and for transmitting

the color signals and the horizontal/vertical synchronous signal in response to

externally-applied predetermined data enable signal and clock signal is met by the

parallel digital data 1 which is covering a total of 12 bits are divided into units each of 3

bits, each unit being inputted to each encoder 10 (Figs. 8 and 9, col. 11, lines 3-26), 2)

the claimed a transmitter that includes a transmitter phase locked loop that, in response

to a clock signal, generates a first plurality of non-overlapping clock signals, the

transmitter for skew-compensating and compressing signals received from the video

controller and for converting the compressed signals to a driving current is met by the

transmitter which includes the encoder 10, the sync pattern adder 11, the input clock

signal 42, the timing pulse generator 30 and the P/S converter 12 (Figs. 8 and 9, col.

11, lines 3-32), 3) the claimed a transmission photo diode for converting the driving

current to an optical signal and for outputting the optical signal is met by the optical

transmitters 20 (Figs. 8 and 9, col. 11, lines 32-35), 4) the claimed an optical

transmission line comprised of a predetermined number of channels, for transmitting the

optical signal is met by the optical fibers 21 (Figs. 8 and 9, col. 11, lines 32-35), 5) the

claimed a reception photo diode for converting the optical signal received from the

optical transmission line into a current signal and for outputting the current signal is met

by the optical receivers 22 (Figs. 8 and 9, col. 11, lines 35-37), and 6) the claimed a

receiver that includes a receiver phase locked loop that generates a second plurality of

non-overlapping clock signals in response to a received clock included in the received

optical signal, for converting the current signal into a voltage signal, for decompressing

the voltage signal in response to the second plurality of non-overlapping clock signals,

for compensating for the skew of the voltage and for restoring the original signal is met

by the receiver side and the decoders 19 (Figs. 8 and 9, col. 11, line 37 to col. 14, line

8).

However, Suemura et al explicitly do not disclose the claimed a transmitter phase

locked loop and a receiver phase locked loop, in response to a clock signal, generates a

first plurality of non-overlapping clock signals of different respective phases, at least one

of non-overlapping clock signals having a phase that is the same as a phase of the

received clock, the non-overlapping clock signals each having a frequency that is the

same as a frequency of the received clock.

Danger teaches that as indicated in FIG. 2, from signals at frequency fx of a

crystal, a plurality of signals phase shifted by one n-th of the corresponding period, to

provide respective signals of phase 1, phase 2… and of phase n, then, as represented

in FIG. 3, if the phase-i signal is used to provide one period of signal CLK, phase i+1

signal (or another signal) can be used to generate the next period, in this case, the

accuracy or jitter corresponds to the input signal period divided by the numbers of

phases (Figs. 2 and 3, col. 1, lines 34-53).

Therefore, it would have been obvious to one ordinary skill in the art at the time

of the invention to incorporate the receive clock and the multi-phase clock as taught by

Danger into Suemura et al's system in order to reduce jitter of the data to be

transmitted.

In considering claim 6, Suemura et al discloses all the claimed subject matter,

note 1) the claimed wherein the receiver phase locked loop further generates a clock

signal in response to the received clock included in the received optical signal is met by

the clock extractor 43 which extracts a transmission clock signal 36 form the output of

the optical receiver 22 and the output clock signal 37 (Figs. 8 and 9, col. 11, line 60 to

col. 12, line 19), 2) the claimed an optical receiver for converting current signals

received from the reception photo diode into voltage signals, and for duty-compensating

and level-converting the voltage signals to obtain digitalized signals which are different

channel data is met by the optical receivers 22 (Figs. 8 and 9, col. 11, lines 35-37), 3)

the claimed a data restoration and skew compensation unit for receiving channel data

that has been compressed by the transmitter, for decompressing the compressed data

in response to the plurality of non-overlapping clock signals, and for skew-compensating

the decompressed data to obtain different channel data each having a predetermined

number of bits is met by the skew compensation which includes the synchronization

pattern detectors 16, controller 41 and bit rotator 17 (Fig. 9, col. 12, line 31 to col. 14,

line 8), and 4) the claimed a descrambler for descrambling in response to the direct

current balance information in each of the channel data, so that the low level and high

level of the channel data balance with each other is met by the decoders 19 (Fig. 9, col. 12, line 31 to col. 14, line 8).

In considering claim 8, the combination of Suemura et al and danger discloses all the limitations of the instant invention as discussed in claims 1 and 6 above, except for providing the claimed wherein the optical receiver further comprises a power down controller for powering down the bias circuit so that it does not operate, in response to an externally-applied power down control signal. The capability of using the power down controller is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known of using power down controller into the combination of Suemura et al and danger's system in order to control the power of the bias circuit.

In considering claim 9, note 1) the claimed a first latch unit for latching for latching received serial data in units of n+N-1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to the second plurality of non-overlapping clock signals comprising first through n-th non-overlapped clock signals, and for outputting N n-bit latch state data having the time difference of a predetermined offset there between is met by the serial-to-parallel (S/P) converters 18 which convert the serial data into parallel data (Fig. 9, col. 12, lines 31-66 of Suemura et al), 2) the claimed the second latch unit for latching in parallel the N state data in response to an X-th (1 ≤X ≤n) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals is met by the multi-phase clocks, phase 1, phase 2...and phase n (Figs. 2 and 3, col. 1, lines 34-53 of Danger), and 3) the claimed a synchronizer

for outputting state data from which the synchronous signal is detected, among data

latched by the second latch unit, as restored information data, in response to a

predetermined synchronous existence signal and the X-th non-overlapped clock signal,

each has a predetermined offset so that the clock signals are not overlapped with each

other is met by the AND gate 56 which takes a logical AND operation of the

synchronization pattern group detection signal Sa and the selector 64 which selects

respective one of the ports of the states 0 to 3 (Figs. 9-12, col. 13, line 10 to col. 14, line

8 of Suemura et al).

In considering claim 19, Suemura et al. discloses all the claimed subject matter,

note 1) the claimed a first latch unit for latching for latching received serial data in units

of n+N-1 (where N is a positive integer greater than or equal to 3) bits in parallel in

response to the first through n-th non-overlapped clock signals, and for outputting N n-

bit latch state data having the time difference of a predetermined offset there between is

met by the serial-to-parallel (S/P) converters 18 which convert the serial data into

parallel data (Fig. 9, col. 12, lines 31-66), 2) the claimed the second latch unit for

latching in parallel the N state data in response to clock signal is met by the first register

60 and the second register 61 (Figs. 9-11, col. 12, line 59 to col. 13, line 46), and 3) the

claimed a synchronizer for outputting state data from which the synchronous signal is

detected, among data latched by the second latch unit, as restored information data, in

response to a predetermined synchronous existence signal and the X-th non-

overlapped clock signal is met by the AND gate 56 which takes a logical AND operation

of the synchronization pattern group detection signal Sa and the selector 64 which

selects respective one of the ports of the states 0 to 3 (Figs. 9-12, col. 13, line 10 to col. 14, line 8).

However, Suemura et al explicitly do not disclose the claimed the clock signal generates a first plurality of non-overlapping clock signals of different respective phases, at least one of non-overlapping clock signals having a phase that is the same as a phase of the received clock, the first through n-th non-overlapped clock signals each having a frequency that is the same as a frequency of the received clock signal, and the second latch unit for latching in parallel the N state data in response to an X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals.

Danger teaches that as indicated in FIG. 2, from signals at frequency fx of a crystal, a plurality of signals phase shifted by one n-th of the corresponding period, to provide respective signals of phase 1, phase 2... and of phase n, then, as represented in FIG. 3, if the phase-i signal is used to provide one period of signal CLK, phase i+1 signal (or another signal) can be used to generate the next period, in this case, the accuracy or jitter corresponds to the input signal period divided by the numbers of phases (Figs. 2 and 3, col. 1, lines 34-53).

Therefore, it would have been obvious to one ordinary skill in the art at the time of the invention to incorporate the receive clock, the multi-phase clocks as taught by Danger into Suemura et al's system in order to reduce jitter of the data to be transmitted.

In considering claim 20, the claimed wherein the predetermined offset is the width of a unit bit constituting the serial data is met by the serial-to-parallel (S/P) converters 18 which convert the serial data into parallel data (Fig. 9, col. 12, lines 31-66 of Suemura et al).

Claim 23 is rejected for the same reason as discussed in claim 19.

6.   Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suemura et al (US Patent No. 5,887,039) in view of Danger (US Patent No. 5,633,608), as applied to claim 1 above, and further in view of Sakamoto et al (US Patent No. 6,557,110 B2).

In considering claim 2, Suemura et al discloses all the claimed subject matter, note 1) the claimed wherein the transmitter phase locked loop further generates a synchronized clock signal to serve as a clock signal for data transmission in response to the externally-applied clock signal is met by the timing pulse generator 40 which generates a timing signal 30, which is "1" during one of 9 time slots and "0" otherwise and is inputted simultaneously to the 4 synchronization pattern adders 11 (Figs. 8 and 9, col. 11, lines 27-35), 2) the claimed a skew compensator for receiving data, each data having a predetermined number of bits, from the video controller; in response to the synchronized clock signal, via different channels, and compensating for a skew which is generated between the channel data in response to the synchronized clock signal is met by the synchronization pattern adders 11 in which the data are written in synchronism to the input clock signal 35 and read out in synchronism to the low frequency clock signal 38 (Figs. 8 and 9, col. 11, lines 3-35), 3) the claimed a data

serialization unit for compressing the scrambled channel data in response to the

synchronized clock signal to obtain 1-bit channel data is met by the P/S converters 12

(Figs. 8 and 9, col. 11, lines 3-35), and 4) the claimed an optical driver for receiving the

compressed channel data and the clock signal as different channel data and converting

the received data into current signals, in order to drive the transmission photo diode is

met by the optical transmitters 20 (Figs. 8 and 9, col. 11, lines 32-35).

However, the combination of Suemura et al and danger explicitly do not disclose

the claimed a scrambler for counting the number of high levels and the number of low

levels of each of the skew-compensated channel data, and adding the counted

information to each of the channel data to serve as direct current balance information,

and transmitting the resultant data.

Sakamoto et al teach that counter circuit 123 begins counting upon receiving a

start signal Scs and stops counting upon receiving a reset signal Scr, as illustrated in

Figs. 7 and 8, counter circuit 123 outputs reference timing signals Sref at a period to

match the frame length, the contents of the shift registers 121 are transferred to data

latch 122 at an output timing given by the reference timing signals Sref (Fig. 5, col. 15,

line 40 to col. 16, line 35).

Therefore, it would have been obvious to one of ordinary skill in the art at the

time of the invention to incorporate the counter as taught by Sakamoto et al into the

combination of Suemura et al and Danger's system in order to provide a channel-to-

channel skew compensation apparatus that can prevent outputting erroneous data.

Allowable Subject Matter

7.   Claims 3-5, 7 and 21-22 are objected to as being dependent upon a rejected

base claim, but would be allowable if rewritten in independent form including all of the

limitations of the base claim and any intervening claims.

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Trang U. Tran whose telephone number is (571) 272-

7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TT
July 20, 2006

Trang U. Tran
Examiner
Art Unit 2622